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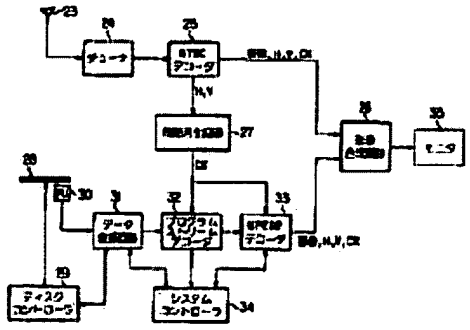
(54) PICTURE DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To attain multiscreen display with easy control without deteriorating picture quality with simple configuration by phase-synchronizing a second system clock used in a second decoding means with a synchronizing signal contained in a first picture signal.
SOLUTION: TV broadcasting wave received by an antenna 23 is supplied to an NTSC decoder 25. A synchronization reproducing circuit 27 generates the system clock CK which is phase-synchronized with a horizontal synchronizing signal H is reproduced by the decoder 25. Picture data recorded in a digital video disk 28 is read, a picture component is supplied to an MPEG 2 decoder 33 and a decoding processing is executed based on the system clock CK so as to be converted into the picture signal. Therefore, the picture signal outputted from the decoder 33 becomes the one which is phase-synchronized with the horizontal synchronizing signal H of the picture signal outputted from the decoder 25.



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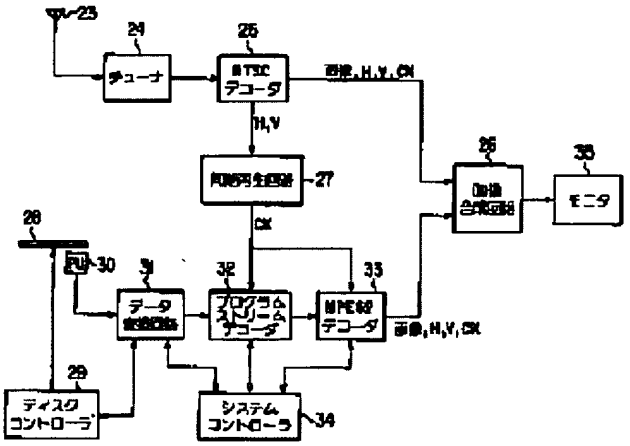
Abstract:
PROBLEM TO BE SOLVED: To attain multiscreen display with easy control without deteriorating picture quality with simple configuration by phase-synchronizing a second system clock used in a second decoding means with a synchronizing signal contained in a first picture signal. SOLUTION: TV broadcasting wave received by an antenna 23 is supplied to an NTSC decoder 25. A synchronization reproducing circuit 27 generates the system clock CK which is phase-synchronized with a horizontal synchronizing signal H is reproduced by the decoder 25. Picture data recorded in a digital video disk 28 is read, a picture component is supplied to an MPEG 2 decoder 33 and a decoding processing is executed based on the system clock CK so as to be converted into the picture signal. Therefore, the picture signal outputted from the decoder 33 becomes the one which is phase-synchronized with the horizontal synchronizing signal H of the picture signal outputted

from the decoder 25.



JPO Machine translation abstract:
(57) **Abstract**
SUBJECT This invention provides the image display device which can moreover perform a multi picture display by easy control, without causing degradation of image quality with simple composition.
Means for Solution The 1st decode means 25 that decodes to the 1st picture signal based on 1st clock CK generated from the synchronized signal H contained in the 1st picture signal, The 2nd decode means 33 that decodes based on 2nd clock CK of different frequency from 1st clock CK to the synchronized signal H contained in the 1st picture signal, and the 2nd picture signal containing the synchronized signal H of the same frequency, The synchronous means 27 to which the synchronized signal H contained in the 1st picture signal is made to carry out phase simulation of the 2nd clock CK used by this 2nd decode means 33, It has the image compositing means 26 which generates a signal for multi picture displays by compounding each signal outputted from the 1st and 2nd decode means 25 and 33 to timing based on the synchronized signal H.

Claim(s)
Claim 1 An image display device comprising:
The 1st decode means that generates the 1st system clock based on a synchronized signal contained in the 1st picture signal, and decodes to said 1st picture signal based on this 1st system clock.
The 2nd decode means that decodes to said 2nd picture signal based on the 2nd system clock of frequency which inputs a synchronized signal contained in said 1st picture signal, and the 2nd picture signal containing a synchronized signal of the same frequency, and is different from said 1st system clock.
A synchronous means to which a synchronized signal contained in said 1st picture signal is made to carry out phase simulation of the 2nd system clock used by this 2nd decode means.

An image compositing means which generates a signal for multi picture displays by compounding each signal outputted from said 1st and 2nd decode means to timing based on said synchronized signal.

Claim 2 The image display device according to claim 1, wherein said synchronous means carries out phase simulation of said 2nd system clock to a Horizontal Synchronizing signal.
Claim 3 The image display device according to claim 2, wherein said 1st system clock has a Horizontal Synchronizing signal 910 times the frequency of said and said 2nd system clock has a Horizontal Synchronizing signal 858 times the frequency of said.

Detailed Description of the Invention
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Field of the Invention The picture signal to which this invention was transmitted, for example by the NTSC (National Television System Committee) method, It is related with the image display device for carrying out the multi picture display of the picture signal read in DVD (Digital Video Disc) on the same screen.
0002
Description of the Prior Art As everyone knows, in recent years, the recording and reproducing system using the recording medium called what is called a DVD which performs compression processing to the digitized dynamic image signal based on progress of the treatment technique of a digital signal and semiconductor technology, and was made to carry out high density recording to an optical disc has been developed. This DVD is the large capacity recording medium whose accommodation of the digital data of 5 G bytes of one side was enabled at the present CD (Compact Disc) and the disk of the equal diameter.
Future development is expected very much.

0003 Drawing 6 shows the reproducing system of this DVD. That is, DVD player 11 shown with the numerals 11 in a figure equipped with DVD12 via the tray 11a provided enabling horizontally free in-and-out, and has changed into the picture signal of NTSC system the image data obtained by performing the reproduction. And image display of the picture signal of the NTSC system outputted from this DVD player 11 comes to be carried out by supplying the television set 14 of a standard method via the cable 13.
0004 As a reproducing system of this DVD12, as shown in drawing 7, the thing of the type which makes the portion of DVD player 11 build in the television set 14 is also considered. Since the portion and the television set 14 of DVD player 11 can share a part of hardware if it does in this way, it can be made advantageous on composition and economy.
0005 Drawing 8 shows the details of this DVD player 11. That is, DVD12 is in the state rotated based on control of the disk controller 15, and the recorded digital image data is read via the optical pick-up 16. After the digital image data read with this optical pick-up 16 is supplied to the data conversion circuit 17 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 18.
0006 This program stream decoder 18 separates the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream, A voice component is outputted to the audio decoder 19, and the image component is outputted to the MPEG(Moving Picture Image Coding Experts Group) 2 decoder 20. And the voice data and the image data to which decoding was performed by this audio decoder 18 and MPEG2 decoder 20, By supplying NTSC encoder 21 and performing encoding processing, it is changed into the picture signal of NTSC system, and is sent out to the above-mentioned cable 13 via the output terminal 22.
0007 By the way, in the above reproducing systems of DVD12. Decoding is performed by the audio decoder 19 and MPEG2 decoder 20 to the data read in DVD12, While causing degradation of image quality since decoding and encoding processing are repeated as NTSC decoding is performed within the television set 14 after encoding processing is performed with NTSC encoder 21, a composition top also has the inconvenience of becoming disadvantageous.
0008 It is not used only in order to display the picture signal outputted from DVD player 11 as the

above-mentioned television set 14, and also in order to receive and carry out image display of the picture signal currently broadcast by usual by the standard (NTSC) method, naturally it is used. That is, both the picture signal outputted from DVD player 11 and the received picture signal will be supplied to this television set 14.

0009 Then, as shown in drawing 9 with a natural thing, the picture signal outputted from DVD player 11 and the received picture signal are compounded, For example, the thing **making a multi picture display perform to the television set 14 so that it may display conversely** comes to be required so that the picture signal outputted from DVD player 11 may be displayed as the parent screen A and the received picture signal may be displayed as the small screen B.

0010 However, the signal which decoded the picture signal read in DVD12, In order to compound the signal which decoded the picture signal of the received NTSC system and to carry out a multi picture display simultaneously, the synthetic circuit of the picture which was adapted for each picture was needed, and the problem that it is necessary to perform complicated control has arisen.

0011 For example, in order to decode the picture signal of NTSC system, the clock which has 4 times as much frequency 4fsc=14.3MHz as the chrominance subcarrier frequency fsc is usually used, but. In order to decode the picture signal read in DVD12, the clock which has the frequency of 13.5 MHz is used. For this reason, complicated control is needed in order to compound both picture signals.

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Problem(s) to be Solved by the Invention As mentioned above, in the reproducing system of the conventional DVD. Since decoding and encoding processing are repeated to the data read in DVD, while causing degradation of image quality, In order to compound the picture signal which decoded the signal read in DVD, and the signal which decoded the picture signal of the received NTSC system and to carry out a multi picture display simultaneously, it has the problem that it is necessary to perform complicated control.

0013 Then, this invention was made in consideration of the above-mentioned situation, and an object of an invention is to provide the very good image display device which can moreover perform a multi picture display by easy control, without causing degradation of image quality with simple composition.

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Means for Solving the Problem The 1st decode means that an image display device concerning this invention generates the 1st system clock based on a synchronized signal contained in the 1st picture signal, and decodes to the 1st picture signal based on this 1st system clock, A synchronized signal contained in the 1st picture signal and the 2nd picture signal containing a synchronized signal of the same frequency are inputted, The 2nd decode means that decodes to the 2nd picture signal based on the 2nd system clock of different frequency from the 1st system clock, A synchronous means to which a synchronized signal contained in the 1st picture signal is made to carry out phase simulation of the 2nd system clock used by this 2nd decode means, By compounding each signal outputted from the 1st and 2nd decode means to timing based on a synchronized signal, it has an image compositing means which generates a signal for multi picture displays.

0015 Moreover, a multi picture display can be performed by easy control, without causing degradation of image quality with simple composition, since it was made to carry out phase simulation of the 2nd system clock used by the 2nd decode means to a synchronized signal contained in the 1st picture signal according to the above composition.

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Embodiment of the Invention Hereafter, this embodiment of the invention is described in detail with reference to Drawings. In drawing 1, the Television Sub-Division broadcast wave received with the antenna 23 is taken out as a baseband signal of NTSC system, when the tuner 24 is supplied and a desired channel tunes in. The baseband signal outputted from this tuner 24 is changed into a picture signal by supplying NTSC decoder 25 and performing decoding.

0017 In this case, in NTSC decoder 25, the chrominance subcarrier fsc is reproduced from the color burst ingredient of the inputted baseband signal, system clock CK which has those 4 times as many frequency 4fsc=14.3MHz is generated, and decoding of a baseband signal is performed. This NTSC decoder 25 is also performing simultaneously reproducing Horizontal Synchronizing signal H and

Vertical Synchronizing signal V from the inputted baseband signal. And both picture signals, Horizontal Synchronizing signals H, Vertical Synchronizing signals V, and system clock CK that were reproduced by this NTSC decoder 25 are supplied to the image compositing circuit 26.
0018 Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were reproduced by above-mentioned NTSC decoder 25 are supplied to the synchronous reproduction circuit 27. This synchronous reproduction circuit 27 is generating system clock CK which has the frequency of 13.5 MHz required in order to decode to the digital image data in which the phase synchronized with Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were inputted, and which is read in DVD28.
0019 On the other hand, this DVD28 is in the state rotated based on control of the disk controller 29, and that recorded digital image data is read via the optical pick-up 30. After the digital image data read with this optical pick-up 30 is supplied to the data conversion circuit 31 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 32.
0020 This program stream decoder 32 has separated the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream based on 13.5-MHz system clock CK generated in the above-mentioned synchronous reproduction circuit 27. In drawing 1, only the image component is shown and it is omitting about the voice component. And the image component outputted from the program stream decoder 32 is supplied to MPEG2 decoder 33, and is changed into a picture signal by performing decoding processing based on 13.5-MHz system clock CK generated in the above-mentioned synchronous reproduction circuit 27.
0021 For this reason, the picture signal outputted from MPEG2 decoder 33 becomes what carried out phase simulation to Horizontal Synchronizing signal H of the picture signal outputted from NTSC decoder 25. That is, the recorded picture is restored by controlling DVD28 by the disk controller 29 and FIFO (First In First Out) which were built in MPEG2 decoder 33 and which is not illustrated.
0022 By then, 13.5-MHz system clock CK which carried out phase simulation to Horizontal Synchronizing signal H of the picture signal outputted from NTSC decoder 25. DVD28 can be reproduced without adding hardware etc. by operating the disk controller 29 and MPEG2 decoder 33.
0023 In this MPEG2 decoder 33, it is also performing simultaneously reproducing Horizontal Synchronizing signal H and Vertical Synchronizing signal V from the inputted image component. And both the picture signal, Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were reproduced by this MPEG2 decoder 33, and system clock CK generated in the synchronous reproduction circuit 27 are supplied to the image compositing circuit 26.
0024 As for the above-mentioned data conversion circuit 31, the program stream decoder 32, and MPEG2 decoder 33, the operation is controlled by the system controller 34. And the described image synthetic circuit 26 compounds the picture signal outputted from NTSC decoder 25, and the picture signal outputted from MPEG2 decoder 33, and is outputting it to the monitor 35.
0025 Drawing 2 shows the details of the above-mentioned synchronous reproduction circuit 27. Namely, 13.5-MHz system clock CK outputted from VCO(Voltage Controlled Oscillator) 36, While being outputted to the above-mentioned program stream decoder 32 and MPEG2 decoder 33 via the output terminal 37, the counter 38 is supplied and dividing is carried out to the frequency of Horizontal Synchronizing signal H.
0026 The phase comparison of system clock CK by which dividing was carried out at this counter 38 is carried out to Horizontal Synchronizing signal H which was supplied to the phase comparison circuit 39 and supplied to the input terminal 40, and that phase error ingredient is outputted to the loop filter 41. And this loop filter 41 generates the direct current voltage corresponding to the inputted phase error ingredient, and 13.5-MHz system clock CK which carried out phase simulation to Horizontal Synchronizing signal H comes to be obtained by controlling the oscillating frequency of above-mentioned VCO36.
0027 Although the phase simulation of 13.5-MHz system clock CK was taken in the above-mentioned synchronous reproduction circuit 27 using Horizontal Synchronizing signal H acquired from NTSC decoder 25, even if this uses the chrominance subcarrier fsc, it becomes possible. In this case, 14.3-MHz system clock CK generated by NTSC decoder 25, 13.5-MHz system clock CK equal 910 times of the frequency Fh of Horizontal Synchronizing signal H and used by MPEG2

decoder 33, The signal which carried out 910 dividing of 14.3-MHz system clock CK generated by NTSC decoder 25 since it was equal **the frequency Fh of Horizontal Synchronizing signal H** 858 times, Phase simulation can be taken by carrying out 858 dividing of 13.5-MHz system clock CK used by MPEG2 decoder 33, and carrying out the phase comparison of the signal.

0028 Next, drawing 3 shows an example of the described image synthetic circuit 26. The picture signal with which the image compositing circuit 26 shown in this drawing 3 is outputted from NTSC decoder 25, The picture signal outputted from MPEG2 decoder 33 is compressed horizontally, respectively, and the image compositing means in the case of making it display on each field which divided the same screen top into two equally horizontally, respectively is shown.

0029 That is, the picture signal outputted from NTSC decoder 25 is written in the memory 43 via the input terminal 42. The picture signal outputted from MPEG2 decoder 33 is written in the memory 45 via the input terminal 44. These memories 43 and 45 have the capacity which all memorizes the data volume for the horizontal pixel number of a picture signal, and writing and read-out of a picture signal are performed based on the timing signal outputted from the controller 46.

0030 This controller 46 is generating the above-mentioned timing signal based on Horizontal Synchronizing signal H supplied to the input terminal 47. Although the frequency of system clock CK of the picture signal supplied to the input terminal 42 is 14.3 MHz and the frequency of system clock CK of the picture signal supplied to the input terminal 44 is 13.5 MHz, Since phase simulation of both system clock CK is carried out, respectively, the relative topology relation of Horizontal Synchronizing signal H is always constant. For this reason, in the memories 43 and 45, both images are compoundable by writing in in the timing of Horizontal Synchronizing signal H, and reading in the timing of same Horizontal Synchronizing signal H.

0031 And with the changeover switch 48 controlled by the controller 46, the picture signal read from both the memories 43 and 45 is selectively taken out by the output terminal 49, and is outputted to said monitor 35. In this case, the picture signal led to the output terminal 49 via the changeover switch 48 since the read timing from both the memories 43 and 45 synchronizes, It becomes that by which two picture signals were compounded horizontally, and the picture signal outputted from NTSC decoder 25 and the picture signal outputted from MPEG2 decoder 33 come to be displayed on each field which divided the screen of the monitor 35 into two equally horizontally, respectively.

0032 Drawing 4 shows other examples of the described image synthetic circuit 26. The image compositing circuit 26 shown in this drawing 4 displays the picture signal outputted from NTSC decoder 25 on the monitor 35 as a parent screen, The image compositing means in the case of displaying the picture signal outputted from MPEG2 decoder 33 all over this parent screen as a small screen, or making that reverse display perform is shown.

0033 That is, the picture signal outputted from NTSC decoder 25 is supplied to the switching circuit 51 via the input terminal 50. The picture signal outputted from MPEG2 decoder 33 is supplied to the switching circuit 51 via the input terminal 52. While this switching circuit 51 leads directly the picture signal supplied to the input terminal 50 to the changeover switch 53, While leading directly the 1st change state that leads the picture signal supplied to the input terminal 52 to the changeover switch 53 via the memory 54, and the picture signal supplied to the input terminal 52 to the changeover switch 53, It is controlled by the 2nd change state that leads the picture signal supplied to the input terminal 50 to the changeover switch 53 via the memory 54.

0034 And the change of such a switching circuit 51, the change of the changeover switch 53, the write-in read operation of the memory 54, etc. are controlled by the controller 56 driven based on Horizontal Synchronizing signal H supplied to the input terminal 55. For this reason, compound a picture signal so that the picture signal which used as the parent screen the picture signal supplied to the input terminal 50, and was supplied to the input terminal 52 may be used as a small screen, or. A picture signal can be compounded so that the picture signal which used as the parent screen the picture signal supplied to the input terminal 52, and was supplied to the input terminal 50 may be used as a small screen, and it can output to the monitor 35 from the output terminal 57.

0035 When an asynchronous picture was originally combined, in consideration of the synchronous relative relation of each picture, needed to change control, but. As mentioned above, a picture is compoundable with very easy composition by carrying out phase simulation of system clock CK of the treating part which decodes each picture beforehand.

0036 Thus, as for the media through a package, the digital broadcasting for which the present broadcast tends to transmit a digital signal by a broadcast wave directly independently is examined independently from now on. At this digital broadcasting, it becomes possible to transmit many channels at once by carrying out Time Division Multiplexing of the compressed picture with the picture into which two or more channels were compressed. And the digital broadcasting decoder currently examined as mentioned above and a DVD player, There are many portions common to composition, and as mentioned above, the television set with a built-in DVD player can reduce hardware scales substantially by considering it as the television set which digital broadcasting can also receive.

0037 Drawing 5 shows the television set which can perform both reception of such digital broadcasting, and reproduction of DVD. That is, the digital broadcasting wave received with the antenna 58 is supplied to the tuner 59, and is changed into a baseband signal. Since the abnormal conditions of QPSK (Quadrature Phase Shift Keying) etc. are usually performed to the baseband signal outputted from this tuner 59, it has changed into the binary signal from the multi valued signal by the demodulator circuit 60.

0038 And since multiplex **of two or more channels** is carried out, the digital signal changed into the binary signal in the demodulator circuit 60 is divided into an image component and a voice component after the signal of a predetermined channel is extracted by the transport stream decoder 61. Among these, sound reproduction is presented with a voice component by the loudspeaker 64, after the audio decoder 63 is supplied via the changeover switch 62 and decoding is performed.

0039 The clock reproduction circuit 66 where a described image ingredient is supplied to MPEG2 decoder 65 and the clock reproduction circuit 66, respectively is generating 13.5-MHz system clock CK required for decoding of the inputted image component. And by performing decoding based on system clock CK to the inputted image component, MPEG2 decoder 65 generates a picture signal, Horizontal Synchronizing signal H, and Vertical Synchronizing signal V, respectively, and is outputting them to the image compositing circuit 67. System clock CK outputted from the clock reproduction circuit 66 is also supplied to the image compositing circuit 67.

0040 On the other hand, the numerals 68 are DVDs, it is in the state rotated based on control of the disk controller 69, and the recorded digital image data is read via the optical pick-up 70. After the digital image data read with this optical pick-up 70 is supplied to the data conversion circuit 71 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 72.

0041 This program stream decoder 72 has separated the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream based on 13.5-MHz system clock CK generated in the above-mentioned clock reproduction circuit 66. Among these, a voice component is supplied to the audio decoder 63 via the above-mentioned changeover switch 62, and sound reproduction is presented with it. By supplying an image component to MPEG2 decoder 73, and performing decoding processing based on 13.5-MHz system clock CK generated in the above-mentioned clock reproduction circuit 66, A picture signal, Horizontal Synchronizing signal H, and Vertical Synchronizing signal V are generated, respectively, and are outputted to the image compositing circuit 67.

0042 And the described image synthetic circuit 67 compounds each picture signal outputted from MPEG2 decoders 65 and 73 to multi picture displays, outputs it to the monitor 74, and it is made to carry out image display. That is, in the television set which reproduces digital broadcasting and DVD68 simultaneously, 13.5-MHz system clock CK generated from the digital broadcasting wave can be used for reproduction of DCD68 as it is, and hardware scales can be reduced substantially. This invention is not limited to the above-mentioned embodiment, in the range which does not deviate from that gist in this outside, can change variously and can be carried out.

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Effect of the Invention The very good image display device which can moreover perform a multi picture display by easy control can be provided without causing degradation of image quality with simple composition according to this invention, as explained in full detail above.

Field of the Invention The picture signal to which this invention was transmitted, for example by the NTSC (National Television System Committee) method, It is related with the image display device for carrying out the multi picture display of the picture signal read in DVD (Digital Video Disc) on the same screen.

Description of the Prior Art As everyone knows, in recent years, the recording and reproducing system using the recording medium called what is called a DVD which performs compression processing to the digitized dynamic image signal based on progress of the treatment technique of a digital signal and semiconductor technology, and was made to carry out high density recording to an optical disc has been developed. It is the large capacity recording medium whose accommodation of the digital data of 5 G bytes of one side this DVD enabled at the present CD (Compact Disc) and the disk of the equal diameter, and future development is expected very much.

0003 Drawing 6 shows the reproducing system of this DVD. That is, DVD player 11 shown with the numerals 11 in a figure equipped with DVD12 via the tray 11a provided enabling horizontally free in-and-out, and has changed into the picture signal of NTSC system the image data obtained by performing the reproduction. And image display of the picture signal of the NTSC system outputted from this DVD player 11 comes to be carried out by supplying the television set 14 of a standard method via the cable 13.
0004 As a reproducing system of this DVD12, as shown in drawing 7, the thing of the type which makes the portion of DVD player 11 build in the television set 14 is also considered. Since the portion and the television set 14 of DVD player 11 can share a part of hardware if it does in this way, it can be made advantageous on composition and economy.
0005 Drawing 8 shows the details of this DVD player 11. That is, DVD12 is in the state rotated based on control of the disk controller 15, and the recorded digital image data is read via the optical pick-up 16. After the digital image data read with this optical pick-up 16 is supplied to the data conversion circuit 17 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 18.
0006 This program stream decoder 18 separates the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream, A voice component is outputted to the audio decoder 19, and the image component is outputted to the MPEG(Moving Picture Image Coding Experts Group) 2 decoder 20. And the voice data and the image data to which decoding was performed by this audio decoder 18 and MPEG2 decoder 20, By supplying NTSC encoder 21 and performing encoding processing, it is changed into the picture signal of NTSC system, and is sent out to the above-mentioned cable 13 via the output terminal 22.
0007 By the way, in the above reproducing systems of DVD12. Decoding is performed by the audio decoder 19 and MPEG2 decoder 20 to the data read in DVD12, While causing degradation of image quality since decoding and encoding processing are repeated as NTSC decoding is performed within the television set 14 after encoding processing is performed with NTSC encoder 21, a composition top also has the inconvenience of becoming disadvantageous.
0008 It is not used only in order to display the picture signal outputted from DVD player 11 as the above-mentioned television set 14, and also in order to receive and carry out image display of the picture signal currently broadcast by usual by the standard (NTSC) method, naturally it is used. That is, both the picture signal outputted from DVD player 11 and the received picture signal will be supplied to this television set 14.
0009 Then, as shown in drawing 9 with a natural thing, the picture signal outputted from DVD player 11 and the received picture signal are compounded, For example, the thing **making a multi picture display perform to the television set 14 so that it may display conversely** comes to be required so that the picture signal outputted from DVD player 11 may be displayed as the parent screen A and the received picture signal may be displayed as the small screen B.
0010 However, the signal which decoded the picture signal read in DVD12, In order to compound the signal which decoded the picture signal of the received NTSC system and to carry out a multi picture display simultaneously, the synthetic circuit of the picture which was adapted for each picture was needed, and the problem that it is necessary to perform complicated control has

arisen.
0011 For example, in order to decode the picture signal of NTSC system, the clock which has 4 times as much frequency 4fsc=14.3MHz as the chrominance subcarrier frequency fsc is usually used, but. In order to decode the picture signal read in DVD12, the clock which has the frequency of 13.5 MHz is used. For this reason, complicated control is needed in order to compound both picture signals.

Effect of the Invention The very good image display device which can moreover perform a multi picture display by easy control can be provided without causing degradation of image quality with simple composition according to this invention, as explained in full detail above.

Problem(s) to be Solved by the Invention As mentioned above, in the reproducing system of the conventional DVD. Since decoding and encoding processing are repeated to the data read in DVD, while causing degradation of image quality, In order to compound the picture signal which decoded the signal read in DVD, and the signal which decoded the picture signal of the received NTSC system and to carry out a multi picture display simultaneously, it has the problem that it is necessary to perform complicated control.
0013 Then, this invention was made in consideration of the above-mentioned situation, and an object of an invention is to provide the very good image display device which can moreover perform a multi picture display by easy control, without causing degradation of image quality with simple composition.

Means for Solving the Problem The 1st decode means that an image display device concerning this invention generates the 1st system clock based on a synchronized signal contained in the 1st picture signal, and decodes to the 1st picture signal based on this 1st system clock, A synchronized signal contained in the 1st picture signal and the 2nd picture signal containing a synchronized signal of the same frequency are inputted, The 2nd decode means that decodes to the 2nd picture signal based on the 2nd system clock of different frequency from the 1st system clock, A synchronous means to which a synchronized signal contained in the 1st picture signal is made to carry out phase simulation of the 2nd system clock used by this 2nd decode means, By compounding each signal outputted from the 1st and 2nd decode means to timing based on a synchronized signal, it has an image compositing means which generates a signal for multi picture displays.
0015 Moreover, a multi picture display can be performed by easy control, without causing degradation of image quality with simple composition, since it was made to carry out phase simulation of the 2nd system clock used by the 2nd decode means to a synchronized signal contained in the 1st picture signal according to the above composition.
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Embodiment of the Invention Hereafter, this embodiment of the invention is described in detail with reference to Drawings. In drawing 1, the Television Sub-Division broadcast wave received with the antenna 23 is taken out as a baseband signal of NTSC system, when the tuner 24 is supplied and a desired channel tunes in. The baseband signal outputted from this tuner 24 is changed into a picture signal by supplying NTSC decoder 25 and performing decoding.
0017 In this case, in NTSC decoder 25, the chrominance subcarrier fsc is reproduced from the color burst ingredient of the inputted baseband signal, system clock CK which has those 4 times as many frequency 4fsc=14.3MHz is generated, and decoding of a baseband signal is performed. This NTSC decoder 25 is also performing simultaneously reproducing Horizontal Synchronizing signal H and Vertical Synchronizing signal V from the inputted baseband signal. And both picture signals, Horizontal Synchronizing signals H, Vertical Synchronizing signals V, and system clock CK that were reproduced by this NTSC decoder 25 are supplied to the image compositing circuit 26.

0018 Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were reproduced by above-mentioned NTSC decoder 25 are supplied to the synchronous reproduction circuit 27. This synchronous reproduction circuit 27 is generating system clock CK which has the frequency of 13.5 MHz required in order to decode to the digital image data in which the phase synchronized with Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were inputted, and which is read in DVD28.
0019 On the other hand, this DVD28 is in the state rotated based on control of the disk controller 29, and that recorded digital image data is read via the optical pick-up 30. After the digital image data read with this optical pick-up 30 is supplied to the data conversion circuit 31 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 32.
0020 This program stream decoder 32 has separated the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream based on 13.5-MHz system clock CK generated in the above-mentioned synchronous reproduction circuit 27. In drawing 1, only the image component is shown and it is omitting about the voice component. And the image component outputted from the program stream decoder 32 is supplied to MPEG2 decoder 33, and is changed into a picture signal by performing decoding processing based on 13.5-MHz system clock CK generated in the above-mentioned synchronous reproduction circuit 27.
0021 For this reason, the picture signal outputted from MPEG2 decoder 33 becomes what carried out phase simulation to Horizontal Synchronizing signal H of the picture signal outputted from NTSC decoder 25. That is, the recorded picture is restored by controlling DVD28 by the disk controller 29 and FIFO (First In First Out) which were built in MPEG2 decoder 33 and which is not illustrated.
0022 By then, 13.5-MHz system clock CK which carried out phase simulation to Horizontal Synchronizing signal H of the picture signal outputted from NTSC decoder 25. DVD28 can be reproduced without adding hardware etc. by operating the disk controller 29 and MPEG2 decoder 33.
0023 In this MPEG2 decoder 33, it is also performing simultaneously reproducing Horizontal Synchronizing signal H and Vertical Synchronizing signal V from the inputted image component. And both the picture signal, Horizontal Synchronizing signal H and Vertical Synchronizing signal V which were reproduced by this MPEG2 decoder 33, and system clock CK generated in the synchronous reproduction circuit 27 are supplied to the image compositing circuit 26.
0024 As for the above-mentioned data conversion circuit 31, the program stream decoder 32, and MPEG2 decoder 33, the operation is controlled by the system controller 34. And the described image synthetic circuit 26 compounds the picture signal outputted from NTSC decoder 25, and the picture signal outputted from MPEG2 decoder 33, and is outputting it to the monitor 35.
0025 Drawing 2 shows the details of the above-mentioned synchronous reproduction circuit 27. Namely, 13.5-MHz system clock CK outputted from VCO(Voltage Controlled Oscillator) 36, While being outputted to the above-mentioned program stream decoder 32 and MPEG2 decoder 33 via the output terminal 37, the counter 38 is supplied and dividing is carried out to the frequency of Horizontal Synchronizing signal H.
0026 The phase comparison of system clock CK by which dividing was carried out at this counter 38 is carried out to Horizontal Synchronizing signal H which was supplied to the phase comparison circuit 39 and supplied to the input terminal 40, and that phase error ingredient is outputted to the loop filter 41. And this loop filter 41 generates the direct current voltage corresponding to the inputted phase error ingredient, and 13.5-MHz system clock CK which carried out phase simulation to Horizontal Synchronizing signal H comes to be obtained by controlling the oscillating frequency of above-mentioned VCO36.
0027 Although the phase simulation of 13.5-MHz system clock CK was taken in the above-mentioned synchronous reproduction circuit 27 using Horizontal Synchronizing signal H acquired from NTSC decoder 25, even if this uses the chrominance subcarrier fsc, it becomes possible. In this case, 14.3-MHz system clock CK generated by NTSC decoder 25, 13.5-MHz system clock CK equal 910 times of the frequency Fh of Horizontal Synchronizing signal H and used by MPEG2 decoder 33, The signal which carried out 910 dividing of 14.3-MHz system clock CK generated by NTSC decoder 25 since it was equal **the frequency Fh of Horizontal Synchronizing signal H** 858 times, Phase simulation can be taken by carrying out 858 dividing of 13.5-MHz system clock

CK used by MPEG2 decoder 33, and carrying out the phase comparison of the signal.
0028 Next, drawing 3 shows an example of the described image synthetic circuit 26. The picture signal with which the image compositing circuit 26 shown in this drawing 3 is outputted from NTSC decoder 25, The picture signal outputted from MPEG2 decoder 33 is compressed horizontally, respectively, and the image compositing means in the case of making it display on each field which divided the same screen top into two equally horizontally, respectively is shown.
0029 That is, the picture signal outputted from NTSC decoder 25 is written in the memory 43 via the input terminal 42. The picture signal outputted from MPEG2 decoder 33 is written in the memory 45 via the input terminal 44. These memories 43 and 45 have the capacity which all memorizes the data volume for the horizontal pixel number of a picture signal, and writing and read-out of a picture signal are performed based on the timing signal outputted from the controller 46.
0030 This controller 46 is generating the above-mentioned timing signal based on Horizontal Synchronizing signal H supplied to the input terminal 47. Although the frequency of system clock CK of the picture signal supplied to the input terminal 42 is 14.3 MHz and the frequency of system clock CK of the picture signal supplied to the input terminal 44 is 13.5 MHz, Since phase simulation of both system clock CK is carried out, respectively, the relative topology relation of Horizontal Synchronizing signal H is always constant. For this reason, in the memories 43 and 45, both images are compoundable by writing in in the timing of Horizontal Synchronizing signal H, and reading in the timing of same Horizontal Synchronizing signal H.
0031 And with the changeover switch 48 controlled by the controller 46, the picture signal read from both the memories 43 and 45 is selectively taken out by the output terminal 49, and is outputted to said monitor 35. In this case, the picture signal led to the output terminal 49 via the changeover switch 48 since the read timing from both the memories 43 and 45 synchronizes, It becomes that by which two picture signals were compounded horizontally, and the picture signal outputted from NTSC decoder 25 and the picture signal outputted from MPEG2 decoder 33 come to be displayed on each field which divided the screen of the monitor 35 into two equally horizontally, respectively.
0032 Drawing 4 shows other examples of the described image synthetic circuit 26. The image compositing circuit 26 shown in this drawing 4 displays the picture signal outputted from NTSC decoder 25 on the monitor 35 as a parent screen, The image compositing means in the case of displaying the picture signal outputted from MPEG2 decoder 33 all over this parent screen as a small screen, or making that reverse display perform is shown.
0033 That is, the picture signal outputted from NTSC decoder 25 is supplied to the switching circuit 51 via the input terminal 50. The picture signal outputted from MPEG2 decoder 33 is supplied to the switching circuit 51 via the input terminal 52. While this switching circuit 51 leads directly the picture signal supplied to the input terminal 50 to the changeover switch 53, While leading directly the 1st change state that leads the picture signal supplied to the input terminal 52 to the changeover switch 53 via the memory 54, and the picture signal supplied to the input terminal 52 to the changeover switch 53, It is controlled by the 2nd change state that leads the picture signal supplied to the input terminal 50 to the changeover switch 53 via the memory 54.
0034 And the change of such a switching circuit 51, the change of the changeover switch 53, the write-in read operation of the memory 54, etc. are controlled by the controller 56 driven based on Horizontal Synchronizing signal H supplied to the input terminal 55. For this reason, compound a picture signal so that the picture signal which used as the parent screen the picture signal supplied to the input terminal 50, and was supplied to the input terminal 52 may be used as a small screen, or. A picture signal can be compounded so that the picture signal which used as the parent screen the picture signal supplied to the input terminal 52, and was supplied to the input terminal 50 may be used as a small screen, and it can output to the monitor 35 from the output terminal 57.
0035 When an asynchronous picture was originally combined, in consideration of the synchronous relative relation of each picture, needed to change control, but. As mentioned above, a picture is compoundable with very easy composition by carrying out phase simulation of system clock CK of the treating part which decodes each picture beforehand.
0036 Thus, as for the media through a package, the digital broadcasting for which the present broadcast tends to transmit a digital signal by a broadcast wave directly independently is examined independently from now on. At this digital broadcasting, it becomes possible to transmit many

channels at once by carrying out Time Division Multiplexing of the compressed picture with the picture into which two or more channels were compressed. And the digital broadcasting decoder currently examined as mentioned above and a DVD player, There are many portions common to composition, and as mentioned above, the television set with a built-in DVD player can reduce hardware scales substantially by considering it as the television set which digital broadcasting can also receive.

0037 Drawing 5 shows the television set which can perform both reception of such digital broadcasting, and reproduction of DVD. That is, the digital broadcasting wave received with the antenna 58 is supplied to the tuner 59, and is changed into a baseband signal. Since the abnormal conditions of QPSK (Quadrature Phase Shift Keying) etc. are usually performed to the baseband signal outputted from this tuner 59, it has changed into the binary signal from the multi valued signal by the demodulator circuit 60.

0038 And since multiplex **of two or more channels** is carried out, the digital signal changed into the binary signal in the demodulator circuit 60 is divided into an image component and a voice component after the signal of a predetermined channel is extracted by the transport stream decoder 61. Among these, sound reproduction is presented with a voice component by the loudspeaker 64, after the audio decoder 63 is supplied via the changeover switch 62 and decoding is performed.

0039 The clock reproduction circuit 66 where a described image ingredient is supplied to MPEG2 decoder 65 and the clock reproduction circuit 66, respectively is generating 13.5-MHz system clock CK required for decoding of the inputted image component. And by performing decoding based on system clock CK to the inputted image component, MPEG2 decoder 65 generates a picture signal, Horizontal Synchronizing signal H, and Vertical Synchronizing signal V, respectively, and is outputting them to the image compositing circuit 67. System clock CK outputted from the clock reproduction circuit 66 is also supplied to the image compositing circuit 67.

0040 On the other hand, the numerals 68 are DVDs, it is in the state rotated based on control of the disk controller 69, and the recorded digital image data is read via the optical pick-up 70. After the digital image data read with this optical pick-up 70 is supplied to the data conversion circuit 71 and changed into the Digital Stream signal of a predetermined format, it is supplied to the program stream decoder 72.

0041 This program stream decoder 72 has separated the voice component and image component by which Time Division Multiplexing was carried out into the inputted stream based on 13.5-MHz system clock CK generated in the above-mentioned clock reproduction circuit 66. Among these, a voice component is supplied to the audio decoder 63 via the above-mentioned changeover switch 62, and sound reproduction is presented with it. By supplying an image component to MPEG2 decoder 73, and performing decoding processing based on 13.5-MHz system clock CK generated in the above-mentioned clock reproduction circuit 66, A picture signal, Horizontal Synchronizing signal H, and Vertical Synchronizing signal V are generated, respectively, and are outputted to the image compositing circuit 67.

0042 And the described image synthetic circuit 67 compounds each picture signal outputted from MPEG2 decoders 65 and 73 to multi picture displays, outputs it to the monitor 74, and it is made to carry out image display. That is, in the television set which reproduces digital broadcasting and DVD68 simultaneously, 13.5-MHz system clock CK generated from the digital broadcasting wave can be used for reproduction of DCD68 as it is, and hardware scales can be reduced substantially. This invention is not limited to the above-mentioned embodiment, in the range which does not deviate from that gist in this outside, can change variously and can be carried out.

0043

Brief Description of the Drawings

Drawing 1 The block lineblock diagram showing the embodiment of the image display device concerning this invention.

Drawing 2 The block lineblock diagram showing the details of the synchronous reproduction circuit in the embodiment.

Drawing 3 The block lineblock diagram showing an example of the image compositing circuit in the

embodiment.
Drawing 4 The block lineblock diagram showing other examples of the image compositing circuit in the embodiment.
Drawing 5 The block lineblock diagram showing other embodiments of this invention.
Drawing 6 The perspective view showing an example of the reproducing system of DVD.
Drawing 7 The perspective view showing other examples of the reproducing system of DVD.
Drawing 8 The block lineblock diagram showing the details of a DVD player.
Drawing 9 The front view shown in order to explain a multi picture display.
Description of Notations
11 **-- Television set,** -- A DVD player, 12 -- DVD, 13 -- A cable, 14 15 -- A disk controller, 16 -- Optical pick-up, 17 -- Data conversion circuit, 18 -- A program stream decoder, 19 -- An audio decoder, 20 -- MPEG2 decoder, 21 **-- Tuner,** -- An NTSC encoder, 22 -- An output terminal, 23 -- An antenna, 24 25 -- An NTSC decoder, 26 -- An image compositing circuit, 27 -- Synchronous reproduction circuit, 28 -- DVD, 29 -- A disk controller, 30 -- Optical pick-up, 31 -- A data conversion circuit, 32 -- A program stream decoder, 33 -- MPEG2 decoder, 34 **-- Output terminal,** -- A system controller, 35 -- A monitor, 36 -- VCO, 37 38 **-- Loop filter,** -- A counter, 39 -- A phase comparison circuit, 40 -- An input terminal, 41 42 **-- A memory, 46 / -- Controller,** -- An input terminal, 43 -- A memory, 44 -- An input terminal, 45 47 **-- An input terminal, 51 / -- A switching circuit, 52 / -- An input terminal, 53 / -- A changeover switch, 54 / -- A memory, 55 / -- An input terminal, 56 / -- A controller, 57 / -- An output terminal, 58 / -- An antenna, 59 / -- A tuner, 60 / -- Demodulator circuit,** -- An input terminal, 48 -- A changeover switch, 49 -- An output terminal, 50 61 -- A transport stream decoder, 62 -- A changeover switch, 63 -- Audio decoder, 64 -- A loudspeaker, 65 -- An MPEG2 decoder, 66 -- Clock reproduction circuit, 67 **-- Optical pick-up, 71 / -- A data conversion circuit, 72 / -- A program stream decoder, 73 / -- An MPEG2 decoder, 74 / -- Monitor.** -- An image compositing circuit, 68 -- DVD, 69 -- A disk controller, 70

Drawing 1

For drawings please refer to the original document.

Drawing 2

For drawings please refer to the original document.

Drawing 3

For drawings please refer to the original document.

Drawing 4

For drawings please refer to the original document.

Drawing 5

For drawings please refer to the original document.

Drawing 6

For drawings please refer to the original document.

Drawing 7

For drawings please refer to the original document.

Drawing 8

For drawings please refer to the original document.

Drawing 9

For drawings please refer to the original document.

For drawings please refer to the original document.

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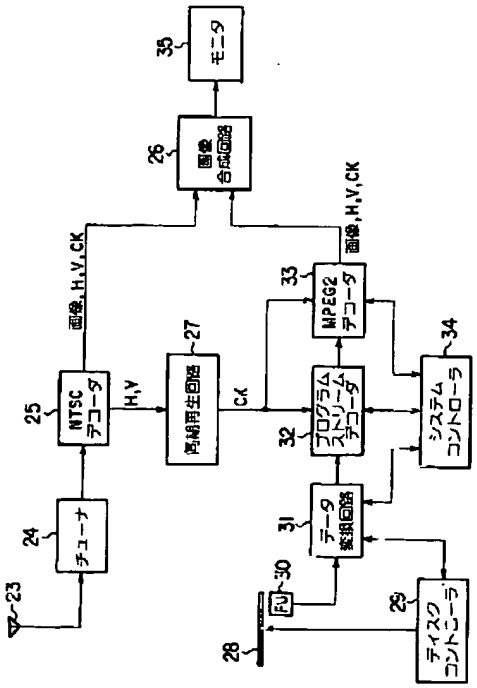
(54)【発明の名称】　画像表示装置

(57)【要約】
【課題】この発明は、簡易な構成で画質の劣化を招くことなく、しかも容易な制御で多画面表示を行ない得る画像表示装置を提供するものである。
【解決手段】第１の画像信号に含まれる同期信号Ｈから生成される第１のクロックＣＫに基づいて第１の画像信号にデコード処理を施す第１のデコード手段２５と、第１の画像信号に含まれる同期信号Ｈと同じ周波数の同期信号Ｈを含む第２の画像信号に、第１のクロックＣＫとは異なる周波数の第２のクロックＣＫに基づいてデコード処理を施す第２のデコード手段３３と、この第２のデコード手段３３で使用される第２のクロックＣＫを、第１の画像信号に含まれる同期信号Ｈに位相同期させる同期手段２７と、第１及び第２のデコード手段２５，３３から出力される各信号を同期信号Ｈに基づくタイミングで合成することにより、多画面表示用の信号を生成する画像合成手段２６とを備えている。



【特許請求の範囲】

【請求項１】　第１の画像信号に含まれる同期信号に基づいて第１のシステムクロックを生成し、この第１のシステムクロックに基づいて前記第１の画像信号にデコード処理を施す第１のデコード手段と、前記第１の画像信号に含まれる同期信号と同じ周波数の同期信号を含む第２の画像信号を入力し、前記第１のシステムクロックとは異なる周波数の第２のシステムクロックに基づいて、前記第２の画像信号にデコード処理を施す第２のデコード手段と、この第２のデコード手段で使用される第２のシステムクロックを、前記第１の画像信号に含まれる同期信号に位相同期させる同期手段と、前記第１及び第２のデコード手段から出力される各信号を前記同期信号に基づくタイミングで合成することにより、多画面表示用の信号を生成する画像合成手段とを具備してなることを特徴とする画像表示装置。

【請求項２】　前記同期手段は、前記第２のシステムクロックを水平同期信号に位相同期させることを特徴とする請求項１記載の画像表示装置。

【請求項３】　前記第１のシステムクロックは前記水平同期信号の９１０倍の周波数を有し、前記第２のシステムクロックは前記水平同期信号の８５８倍の周波数を有することを特徴とする請求項２記載の画像表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は、例えばＮＴＳＣ（National Television System Committee）方式で伝送された画像信号と、ＤＶＤ（Digital Video Disc）から読み取った画像信号とを、同一画面上に多画面表示するための画像表示装置に関する。

【０００２】

【従来の技術】周知のように、近年では、デジタル信号の処理技術や半導体技術の進歩に基づいて、デジタル化された動画像信号に圧縮処理を施して光ディスクに高密度記録するようにした、いわゆるＤＶＤと称される記録媒体を用いた記録再生システムが開発されてきている。このＤＶＤは、現状のＣＤ（Compact Disc）と同径のディスクに、片面５ギガバイトものデジタルデータを収容可能とした大容量記録媒体であり、今後の発展が大いに期待されているものである。

【０００３】図６は、このＤＶＤの再生システムを示している。すなわち、図中符号１１で示すＤＶＤプレーヤ１１は、水平方向に出入自在に設けられるトレイ１１ａを介してＤＶＤ１２を装着し、その再生を行ない、得られた画像データをＮＴＳＣ方式の画像信号に変換している。そして、このＤＶＤプレーヤ１１から出力されたＮＴＳＣ方式の画像信号が、ケーブル１３を介して標準方式のテレビジョン受信機１４に供給されることにより、画像表示されるようになる。

【０００４】なお、このＤＶＤ１２の再生システムとしては、図７に示すように、ＤＶＤプレーヤ１１の部分をテレビジョン受信機１４に内蔵させるタイプのものも考えられている。このようにすれば、ＤＶＤプレーヤ１１の部分とテレビジョン受信機１４とで、ハードウェアの一部を共有することができるようになるため、構成上及び経済上有利にすることができる。

【０００５】図８は、このＤＶＤプレーヤ１１の詳細を示している。すなわち、ＤＶＤ１２は、ディスクコントローラ１５の制御に基づいて回転駆動された状態で、光学式ピックアップ１６を介して、その記録されたデジタル画像データが読み取られる。この光学式ピックアップ１６で読み取られたデジタル画像データは、データ変換回路１７に供給されて所定のフォーマットのデジタルストリーム信号に変換された後、プログラムストリームデコーダ１８に供給される。

【０００６】このプログラムストリームデコーダ１８は、入力されたストリーム中に時分割多重された音声成分と画像成分とを分離し、音声成分を音声デコーダ１９に出力し、画像成分をＭＰＥＧ（Moving Picture Image Coding Experts Group）２デコーダ２０に出力している。そして、この音声デコーダ１８及びＭＰＥＧ２デコーダ２０でデコード処理が施された音声データ及び画像データは、ＮＴＳＣエンコーダ２１に供給されてエンコード処理が施されることにより、ＮＴＳＣ方式の画像信号に変換され、出力端子２２を介して上記ケーブル１３に送出される。

【０００７】ところで、上記のようなＤＶＤ１２の再生システムでは、ＤＶＤ１２から読み取ったデータに対して、音声デコーダ１９やＭＰＥＧ２デコーダ２０によりデコード処理が施され、ＮＴＳＣエンコーダ２１でエンコード処理が施された後、テレビジョン受信機１４内でＮＴＳＣデコード処理が施されるというように、デコード処理とエンコード処理とが繰り返されるので、画質の劣化を招くとともに、構成上も不利になるという不都合がある。

【０００８】また、上記テレビジョン受信機１４としては、ＤＶＤプレーヤ１１から出力された画像信号を表示するためだけに用いられることはなく、通常に標準（ＮＴＳＣ）方式で放送されている画像信号を受信して画像表示するためにも用いられることは当然である。すなわち、このテレビジョン受信機１４には、ＤＶＤプレーヤ１１から出力される画像信号と、受信された画像信号とが共に供給されることになる。

【０００９】すると、当然のことながら、図９に示すように、ＤＶＤプレーヤ１１から出力される画像信号と受信された画像信号とを合成し、例えば、ＤＶＤプレーヤ１１から出力される画像信号を親画面Ａとして表示し、受信された画像信号を小画面Ｂとして表示するように、またはその逆に表示するように、テレビジョン受信機１４に多画面表示を行なわせることが要求されるようにな

る。

【００１０】しかしながら、ＤＶＤ１２から読み取られた画像信号をデコード処理した信号と、受信されたＮＴＳＣ方式の画像信号をデコード処理した信号とを合成して同時に多画面表示するには、それぞれの画像に適応した画像の合成回路が必要となり、複雑な制御を行なう必要があるという問題が生じている。

【００１１】例えば、ＮＴＳＣ方式の画像信号をデコード処理するためには、通常、色副搬送波周波数ｆｓｃの４倍の周波数４ｆｓｃ＝１４．３ＭＨｚを有するクロックが用いられるが、ＤＶＤ１２から読み取られた画像信号をデコード処理するためには、１３．５ＭＨｚの周波数を有するクロックが用いられる。このため、両方の画像信号を合成するには、複雑な制御が必要になる。

【００１２】

【発明が解決しようとする課題】以上のように、従来のＤＶＤの再生システムでは、ＤＶＤから読み取ったデータにデコード処理とエンコード処理とを繰り返しているので画質の劣化を招くとともに、ＤＶＤから読み取った信号をデコード処理した画像信号と、受信されたＮＴＳＣ方式の画像信号をデコード処理した信号とを合成して同時に多画面表示するには、複雑な制御を行なう必要があるという問題を有している。

【００１３】そこで、この発明は上記事情を考慮してなされたもので、簡易な構成で画質の劣化を招くことなく、しかも容易な制御で多画面表示を行ない得る極めて良好な画像表示装置を提供することを目的とする。

【００１４】

【課題を解決するための手段】この発明に係る画像表示装置は、第１の画像信号に含まれる同期信号に基づいて第１のシステムクロックを生成し、この第１のシステムクロックに基づいて第１の画像信号にデコード処理を施す第１のデコード手段と、第１の画像信号に含まれる同期信号と同じ周波数の同期信号を含む第２の画像信号を入力し、第１のシステムクロックとは異なる周波数の第２のシステムクロックに基づいて、第２の画像信号にデコード処理を施す第２のデコード手段と、この第２のデコード手段で使用される第２のシステムクロックを、第１の画像信号に含まれる同期信号に位相同期させる同期手段と、第１及び第２のデコード手段から出力される各信号を同期信号に基づくタイミングで合成することにより、多画面表示用の信号を生成する画像合成手段とを備えるようにしたものである。

【００１５】上記のような構成によれば、第２のデコード手段で使用される第２のシステムクロックを、第１の画像信号に含まれる同期信号に位相同期させるようにしたので、簡易な構成で画質の劣化を招くことなく、しかも容易な制御で多画面表示を行なうことができるようになる。

【００１６】

【発明の実施の形態】以下、この発明の実施の形態について図面を参照して詳細に説明する。図１において、アンテナ２３で受信されたテレビジョン放送波は、チューナ２４に供給されて所望のチャンネルが選局されることにより、ＮＴＳＣ方式のベースバンド信号として取り出される。このチューナ２４から出力されるベースバンド信号は、ＮＴＳＣデコーダ２５に供給されてデコード処理が施されることにより、画像信号に変換される。

【００１７】この場合、ＮＴＳＣデコーダ２５では、入力されたベースバンド信号のカラーバースト成分から色副搬送波ｆｓｃを再生し、その４倍の周波数４ｆｓｃ＝１４．３ＭＨｚを有するシステムクロックＣＫを生成して、ベースバンド信号のデコード処理を実行している。また、このＮＴＳＣデコーダ２５は、入力されたベースバンド信号から、水平同期信号Ｈと垂直同期信号Ｖとを再生することも同時に行なっている。そして、このＮＴＳＣデコーダ２５で再生された画像信号、水平同期信号Ｈ、垂直同期信号Ｖ及びシステムクロックＣＫは、共に画像合成回路２６に供給されている。

【００１８】また、上記ＮＴＳＣデコーダ２５で再生された水平同期信号Ｈ及び垂直同期信号Ｖは、同期再生回路２７に供給される。この同期再生回路２７は、入力された水平同期信号Ｈ及び垂直同期信号Ｖに位相が同期した、ＤＶＤ２８から読み取られるデジタル画像データにデコード処理を施すために必要な１３．５ＭＨｚの周波数を有するシステムクロックＣＫを生成している。

【００１９】一方、このＤＶＤ２８は、ディスクコントローラ２９の制御に基づいて回転駆動された状態で、光学式ピックアップ３０を介して、その記録されたデジタル画像データが読み取られる。この光学式ピックアップ３０で読み取られたデジタル画像データは、データ変換回路３１に供給されて、所定のフォーマットのデジタルストリーム信号に変換された後、プログラムストリームデコーダ３２に供給される。

【００２０】このプログラムストリームデコーダ３２は、上記同期再生回路２７で生成された１３．５ＭＨｚのシステムクロックＣＫに基づいて、入力されたストリーム中に時分割多重された音声成分と画像成分とを分離している。なお、図１では、画像成分についてのみ示しており、音声成分については省略している。そして、プログラムストリームデコーダ３２から出力された画像成分は、ＭＰＥＧ２デコーダ３３に供給され、上記同期再生回路２７で生成された１３．５ＭＨｚのシステムクロックＣＫに基づいて復号化処理が施されることにより、画像信号に変換される。

【００２１】このため、ＭＰＥＧ２デコーダ３３から出力される画像信号は、ＮＴＳＣデコーダ２５から出力される画像信号の水平同期信号Ｈに位相同期したものとなる。つまり、ＤＶＤ２８は、ディスクコントローラ２９や、ＭＰＥＧ２デコーダ３３に内蔵された図示しないＦ

ＩＦＯ（First In First Out）によって制御されることにより、記録された画像が復元される。

【００２２】そこで、ＮＴＳＣデコーダ２５から出力される画像信号の水平同期信号Ｈに位相同期した１３．５ＭＨｚのシステムクロックＣＫで、ディスクコントローラ２９やＭＰＥＧ２デコーダ３３を動作させることにより、ハードウェア等を追加することなく、ＤＶＤ２８の再生を行なうことができる。

【００２３】また、このＭＰＥＧ２デコーダ３３では、入力された画像成分から水平同期信号Ｈと垂直同期信号Ｖとを再生することも同時に行なっている。そして、このＭＰＥＧ２デコーダ３３で再生された画像信号、水平同期信号Ｈ及び垂直同期信号Ｖと、同期再生回路２７で生成されたシステムクロックＣＫとは、共に画像合成回路２６に供給されている。

【００２４】なお、上記データ変換回路３１，プログラムストリームデコーダ３２及びＭＰＥＧ２デコーダ３３は、システムコントローラ３４によって、その動作が制御されている。そして、上記画像合成回路２６は、ＮＴＳＣデコーダ２５から出力された画像信号と、ＭＰＥＧ２デコーダ３３から出力された画像信号とを合成し、モニタ３５に出力している。

【００２５】図２は、上記同期再生回路２７の詳細を示している。すなわち、ＶＣＯ（Voltage Controlled Oscillator）３６から出力される１３．５ＭＨｚのシステムクロックＣＫは、出力端子３７を介して上記プログラムストリームデコーダ３２及びＭＰＥＧ２デコーダ３３に出力されるとともに、カウンタ３８に供給されて水平同期信号Ｈの周波数まで分周される。

【００２６】このカウンタ３８で分周されたシステムクロックＣＫは、位相比較回路３９に供給されて、入力端子４０に供給された水平同期信号Ｈと位相比較され、その位相誤差成分がループフィルタ４１に出力される。そして、このループフィルタ４１が、入力された位相誤差成分に対応した直流電圧を発生して、上記ＶＣＯ３６の発振周波数を制御することにより、水平同期信号Ｈに位相同期した１３．５ＭＨｚのシステムクロックＣＫが得られるようになる。

【００２７】上記した同期再生回路２７では、ＮＴＳＣデコーダ２５から得られる水平同期信号Ｈを用いて、１３．５ＭＨｚのシステムクロックＣＫの位相同期をとるようにしたが、これは例えば色副搬送波ｆｓｃを用いても可能となる。この場合、ＮＴＳＣデコーダ２５で生成される１４．３ＭＨｚのシステムクロックＣＫは、水平同期信号Ｈの周波数Ｆｈの９１０倍に等しく、ＭＰＥＧ２デコーダ３３で使用される１３．５ＭＨｚのシステムクロックＣＫは、水平同期信号Ｈの周波数Ｆｈの８５８倍に等しくなっているので、ＮＴＳＣデコーダ２５で生成された１４．３ＭＨｚのシステムクロックＣＫを９１０分周した信号と、ＭＰＥＧ２デコーダ３３で使用される１３．５ＭＨｚのシステムクロックＣＫを８５８分周して信号とを位相比較することで、位相同期をとることができる。

【００２８】次に、図３は、上記画像合成回路２６の一例を示している。この図３に示される画像合成回路２６は、ＮＴＳＣデコーダ２５から出力される画像信号と、ＭＰＥＧ２デコーダ３３から出力される画像信号とを、それぞれ水平方向に圧縮し、同一画面上を水平方向に２等分した各領域にそれぞれ表示させる場合の画像合成手段を示している。

【００２９】すなわち、ＮＴＳＣデコーダ２５から出力される画像信号は、入力端子４２を介してメモリ４３に書き込まれる。また、ＭＰＥＧ２デコーダ３３から出力される画像信号は、入力端子４４を介してメモリ４５に書き込まれる。これらメモリ４３，４５は、いずれも画像信号の水平方向画素数分のデータ量を記憶する容量を有し、コントローラ４６から出力されるタイミング信号に基づいて、画像信号の書き込みや読み出しが行なわれる。

【００３０】このコントローラ４６は、入力端子４７に供給される水平同期信号Ｈに基づいて、上記タイミング信号を生成している。入力端子４２に供給される画像信号のシステムクロックＣＫの周波数は１４．３ＭＨｚであり、入力端子４４に供給される画像信号のシステムクロックＣＫの周波数は１３．５ＭＨｚであるが、両システムクロックＣＫはそれぞれ位相同期しているため、水平同期信号Ｈの相対位相関係は常に一定となっている。このため、メモリ４３，４５において、水平同期信号Ｈのタイミングで書き込みを行ない、同一の水平同期信号Ｈのタイミングで読み出しを行なうことにより、両画像を合成することができる。

【００３１】そして、両メモリ４３，４５から読み出された画像信号は、コントローラ４６によって制御される切替スイッチ４８によって選択的に出力端子４９に取り出され、前記モニタ３５に出力される。この場合、両メモリ４３，４５からの読み出しタイミングが同期しているため、切替スイッチ４８を介して出力端子４９に導かれる画像信号は、水平方向に２つの画像信号が合成されたものとなり、ＮＴＳＣデコーダ２５から出力される画像信号と、ＭＰＥＧ２デコーダ３３から出力される画像信号とが、モニタ３５の画面を水平方向に２等分した各領域にそれぞれ表示されるようになる。

【００３２】また、図４は、上記画像合成回路２６の他の例を示している。この図４に示される画像合成回路２６は、ＮＴＳＣデコーダ２５から出力される画像信号をモニタ３５に親画面として表示し、この親画面中にＭＰＥＧ２デコーダ３３から出力される画像信号を小画面として表示するか、またはその逆の表示を行なわせる場合の画像合成手段を示している。

【００３３】すなわち、ＮＴＳＣデコーダ２５から出力

される画像信号は、入力端子５０を介してスイッチ回路５１に供給される。また、ＭＰＥＧ２デコーダ３３から出力される画像信号は、入力端子５２を介してスイッチ回路５１に供給される。このスイッチ回路５１は、入力端子５０に供給された画像信号を切替スイッチ５３に直接導くとともに、入力端子５２に供給された画像信号をメモリ５４を介して切替スイッチ５３に導く第１の切替状態と、入力端子５２に供給された画像信号を切替スイッチ５３に直接導くとともに、入力端子５０に供給された画像信号をメモリ５４を介して切替スイッチ５３に導く第２の切替状態とに制御される。

【００３４】そして、このようなスイッチ回路５１の切り替えや、切替スイッチ５３の切り替え及びメモリ５４の書き込み読み出し動作等は、入力端子５５に供給される水平同期信号Ｈに基づいて駆動されるコントローラ５６によって制御されている。このため、入力端子５０に供給された画像信号を親画面とし入力端子５２に供給された画像信号を小画面とするように画像信号を合成したり、入力端子５２に供給された画像信号を親画面とし入力端子５０に供給された画像信号を小画面とするように画像信号を合成して、出力端子５７からモニタ３５に出力することができる。

【００３５】本来、非同期の画像を合成する場合には、それぞれの画像の同期の相対関係を考慮して制御を切り替える必要があったが、以上のように、予めそれぞれの画像をデコードする処理部のシステムクロックＣＫを位相同期させておくことにより、非常に簡単な構成で画像の合成を行なうことができる。

【００３６】このようにパッケージを媒体としたメディアとは別に、今後は、現在の放送とは別にデジタル信号を直接放送波で伝送しようとするデジタル放送が検討されている。このデジタル放送では、圧縮された画像を複数のチャンネルの圧縮された画像とともに時分割多重することで、多数のチャンネルを一度に伝送することが可能となる。そして、以上のように検討されているデジタル放送デコーダと、ＤＶＤプレーヤとは、構成に共通な部分が多く、前述したようにＤＶＤプレーヤ内蔵のテレビジョン受信機は、デジタル放送も受信することのできるテレビジョン受信機とすることでハードウェア規模を大幅に削減することができる。

【００３７】図5は、このようなデジタル放送の受信とＤＶＤの再生とを両方行なうことのできるテレビジョン受信機を示している。すなわち、アンテナ５８で受信されたデジタル放送波は、チューナ５９に供給されてベースバンド信号に変換される。このチューナ５９から出力されるベースバンド信号には、通常ＱＰＳＫ（Quadrature Phase Shift Keying ）等の変調が施されているため、復調回路６０により多値信号から２値信号に変換している。

【００３８】そして、復調回路６０で２値信号に変換されたデジタル信号は、複数のチャンネルが多重されているため、トランスポートストリームデコーダ６１により所定チャンネルの信号が抽出された後、画像成分と音声成分とに分離される。このうち、音声成分は、切替スイッチ６２を介して音声デコーダ６３に供給されデコード処理が施された後、スピーカ６４によって音声再生に供される。

【００３９】また、上記画像成分は、ＭＰＥＧ２デコーダ６５及びクロック再生回路６６にそれぞれ供給される、クロック再生回路６６は、入力された画像成分のデコード処理に必要な１３．５ＭＨｚのシステムクロックＣＫを生成している。そして、ＭＰＥＧ２デコーダ６５は、入力された画像成分にシステムクロックＣＫに基づいたデコード処理を施すことにより、画像信号，水平同期信号Ｈ及び垂直同期信号Ｖをそれぞれ生成して、画像合成回路６７に出力している。なお、クロック再生回路６６から出力されるシステムクロックＣＫも、画像合成回路６７に供給されている。

【００４０】一方、符号６８はＤＶＤであり、ディスクコントローラ６９の制御に基づいて回転駆動された状態で、光学式ピックアップ７０を介して、その記録されたデジタル画像データが読み取られる。この光学式ピックアップ７０で読み取られたデジタル画像データは、データ変換回路７１に供給されて、所定のフォーマットのデジタルストリーム信号に変換された後、プログラムストリームデコーダ７２に供給される。

【００４１】このプログラムストリームデコーダ７２は、上記クロック再生回路６６で生成された１３．５ＭＨｚのシステムクロックＣＫに基づいて、入力されたストリーム中に時分割多重された音声成分と画像成分とを分離している。このうち、音声成分は、上記切替スイッチ６２を介して音声デコーダ６３に供給され、音声再生に供される。また、画像成分は、ＭＰＥＧ２デコーダ７３に供給され、上記クロック再生回路６６で生成された１３．５ＭＨｚのシステムクロックＣＫに基づいて復号化処理が施されることにより、画像信号，水平同期信号Ｈ及び垂直同期信号Ｖがそれぞれ生成され、画像合成回路６７に出力される。

【００４２】そして、上記画像合成回路６７は、ＭＰＥＧ２デコーダ６５，７３から出力された各画像信号を多画面表示用に合成し、モニタ７４に出力して画像表示させるようにしている。すなわち、デジタル放送とＤＶＤ６８とを同時に再生するテレビジョン受信機では、デジタル放送波から生成された１３．５ＭＨｚのシステムクロックＣＫをそのままＤＣＤ６８の再生に用いることができ、ハードウェア規模を大幅に削減することができる。なお、この発明は上記した実施の形態に限定されるものではなく、この外その要旨を逸脱しない範囲で種々変形して実施することができる。

【００４３】

【発明の効果】以上詳述したようにこの発明によれば、簡易な構成で画質の劣化を招くことなく、しかも容易な制御で多画面表示を行ない得る極めて良好な画像表示装置を提供することができる。

【図面の簡単な説明】

【図１】この発明に係る画像表示装置の実施の形態を示すブロック構成図。

【図２】同実施の形態における同期再生回路の詳細を示すブロック構成図。

【図３】同実施の形態における画像合成回路の一例を示すブロック構成図。

【図４】同実施の形態における画像合成回路の他の例を示すブロック構成図。

【図５】この発明の他の実施の形態を示すブロック構成図。

【図６】ＤＶＤの再生システムの一例を示す斜視図。

【図７】ＤＶＤの再生システムの他の例を示す斜視図。

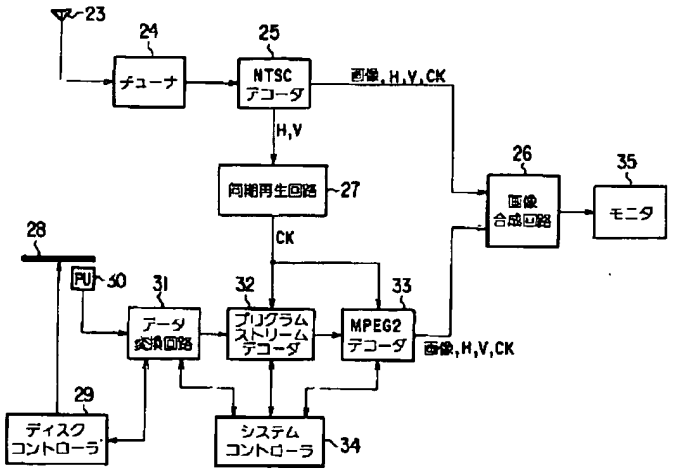
【図８】ＤＶＤプレーヤの詳細を示すブロック構成図。

【図９】多画面表示を説明するために示す正面図。

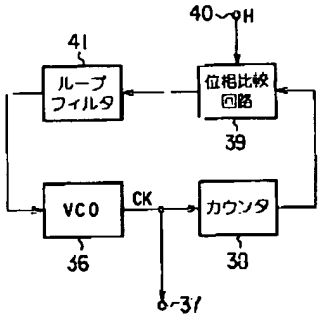
【符号の説明】

１１…ＤＶＤプレーヤ、１２…ＤＶＤ、１３…ケーブル、１４…テレビジョン受信機、１５…ディスクコントローラ、１６…光学式ピックアップ、１７…データ変換回路、１８…プログラムストリームデコーダ、１９…音声デコーダ、２０…ＭＰＥＧ２デコーダ、２１…ＮＴＳＣエンコーダ、２２…出力端子、２３…アンテナ、２４…チューナ、２５…ＮＴＳＣデコーダ、２６…画像合成回路、２７…同期再生回路、２８…ＤＶＤ、２９…ディスクコントローラ、３０…光学式ピックアップ、３１…データ変換回路、３２…プログラムストリームデコーダ、３３…ＭＰＥＧ２デコーダ、３４…システムコントローラ、３５…モニタ、３６…ＶＣＯ、３７…出力端子、３８…カウンタ、３９…位相比較回路、４０…入力端子、４１…ループフィルタ、４２…入力端子、４３…メモリ、４４…入力端子、４５…メモリ、４６…コントローラ、４７…入力端子、４８…切替スイッチ、４９…出力端子、５０…入力端子、５１…スイッチ回路、５２…入力端子、５３…切替スイッチ、５４…メモリ、５５…入力端子、５６…コントローラ、５７…出力端子、５８…アンテナ、５９…チューナ、６０…復調回路、６１…トランスポートストリームデコーダ、６２…切替スイッチ、６３…音声デコーダ、６４…スピーカ、６５…ＭＰＥＧ２デコーダ、６６…クロック再生回路、６７…画像合成回路、６８…ＤＶＤ、６９…ディスクコントローラ、７０…光学式ピックアップ、７１…データ変換回路、７２…プログラムストリームデコーダ、７３…ＭＰＥＧ２デコーダ、７４…モニタ。

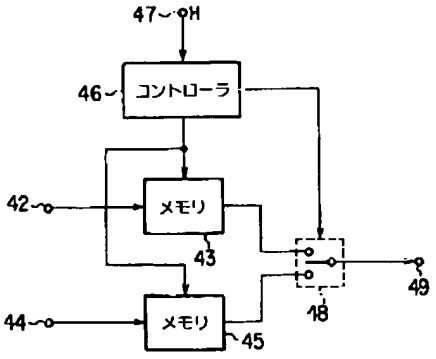
【図1】



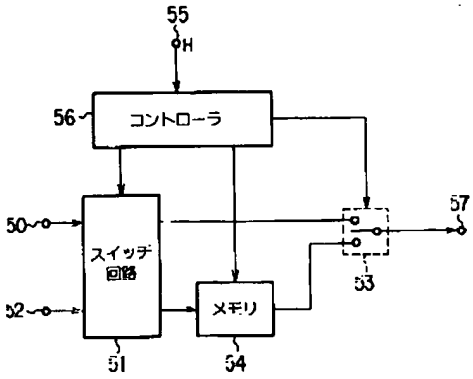
【図2】



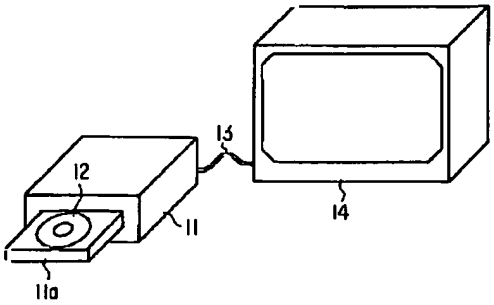
【図3】



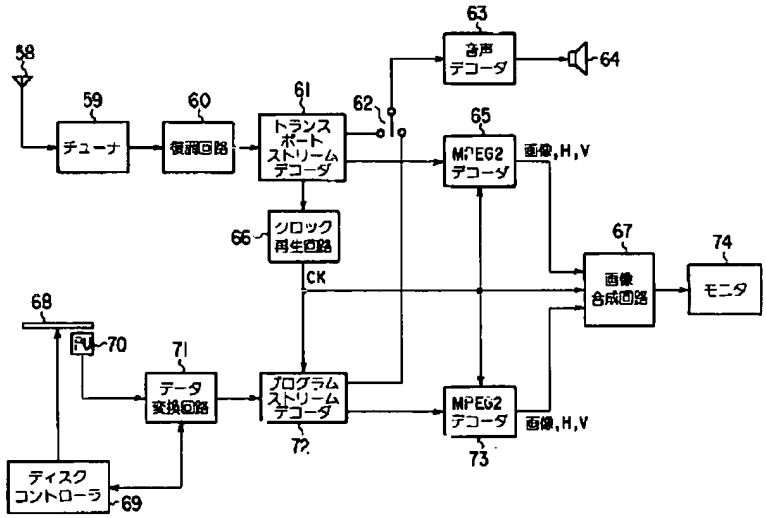
【図4】



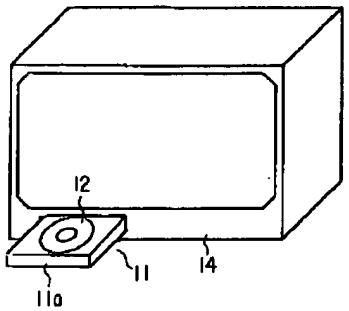
【図6】



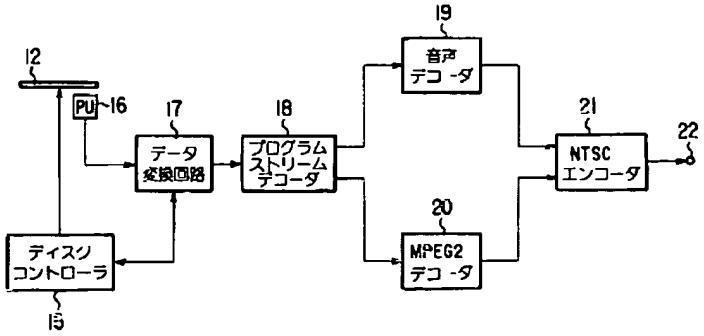
【図5】



【図7】



【図8】



【図9】